## AMENDMENTS TO THE CLAIMS

The following listing of claims replaces all prior listings of claims in the present application.

What is claimed is:

**1. (Canceled)**

**2. (Currently Amended)** A memory module comprising a plurality of memory devices, which share a bus line, on a board,

wherein the bus line connects terminals of said plurality of memory devices in a stubless configuration and an end of said bus line is terminated, [[and]]

wherein at least a part of said bus line is a strip line,

wherein at least one of said plurality of memory devices is a memory device in which a termination circuit is included, and

wherein the memory device in which said termination circuit is included terminates the end of said bus line.

**3. (Previously Presented)** The memory module as defined by claim 2, wherein an effective characteristic impedance of said bus line is matched with a characteristic impedance of a line on a motherboard on which said memory module is mounted.

**4-6. (Canceled)**

**7. (Currently Amended)** A [[The]] memory module ~~as defined by claim 2,~~ comprising a plurality of memory devices, which share a bus line, on a board,

wherein the bus line connects terminals of said plurality of memory devices in a stubless configuration and an end of said bus line is terminated,

wherein at least a part of said bus line is a strip line,

wherein at least one of the plurality of memory devices comprises an on-chip terminator terminating said bus line by turning on a transfer gate that is provided between one end of a termination resistor and a termination voltage, the other end of the termination resistor being connected to the terminal of said memory device connected to said bus line.

**8. (Currently Amended)** A [[The]] memory module ~~as defined by claim 2:~~ comprising a plurality of memory devices, which share a bus line, on a board,

wherein the bus line connects terminals of said plurality of memory devices in a stubless configuration and an end of said bus line is terminated,

wherein at least a part of said bus line is a strip line,

wherein at least one of the plurality of memory devices comprises an on-chip terminator comprising a first transfer gate and a second transfer gate and terminating said bus line by turning on said first transfer gate and said second transfer gate,

wherein said first transfer gate is connected between one end of a first termination resistor and a high-potential power supply voltage, the other end of the first termination resistor being connected to the terminal of said memory device connected to said bus line, and

wherein said second transfer gate is connected between one end of a second termination resistor and a low-potential power supply voltage, the other end of the second termination resistor

being connected to the terminal of said memory device connected to said bus line.

**9. (Original)** A memory module comprising a board on which a plurality of memory devices, which share a bus line, are mounted on a front surface and a back surface,

wherein said bus line is extended on the front surface of said board from a first module terminal to a via hole spaced from said first module terminal and is connected to one end of a first strip line through the via hole,

wherein terminals of the memory devices mounted on the front surface of the board are connected to said first strip line each through a via hole,

wherein said first strip line is extended in one direction and the other end, which is an end opposite to said one end, is connected to one end of a second strip line through a loop-back via hole,

wherein said second strip line is extended in a direction opposite to said one direction,

wherein terminals of the memory devices mounted on the back surface of the board are connected to said second strip line each through a via hole,

wherein a termination circuit is provided near a second module terminal on the back surface of the board, and

wherein said termination circuit is connected through a via hole to the other end of said second strip line that is looped.

**10. (Original)** The memory module as defined by claim 9 wherein, near a loop-back point of said bus line, a power supply layer and a ground layer, between which said strip line forming said bus line is provided, are connected by a bypass capacitor and/or common power supply layers or

ground layers are shorted.

**11. (Previously Presented)** The memory module as defined by claim 2, wherein signal terminals of said plurality of memory devices connected in the stubless configuration are connected at one point on the bus.

**12-14. (Canceled)**

**15. (Currently Amended)** A [[The]] memory module ~~as defined by claim 2,~~ comprising a plurality of memory devices, which share a bus line, on a board,

wherein the bus line connects terminals of said plurality of memory devices in a stubless configuration and an end of said bus line is terminated,

wherein at least a part of said bus line is a strip line, and

wherein a register, connected to said bus line for converting signals, is provided on the board of said memory module.

**16. (Canceled)**

**17. (Currently Amended)** The memory module as defined by claim 2:

wherein said memory devices each have a package board that makes an electrical connection between a memory chip pad and said board, and

wherein said package board has a strip line for use as a signal line of said bus line in said package board.

**18. (Previously Presented)** The memory module as defined by claim 2, wherein said memory module is configured as a multi-chip module.

**19. (Previously Presented)** The memory module as defined by claim 2, wherein the board of said memory module is divided into a plurality of boards and said plurality of boards are each connected by inter-board connection means.

**20. (Canceled)**

**21. (Currently Amended)** A [[The]] memory module ~~as defined by claim 2:~~ comprising a plurality of memory devices, which share a bus line, on a board,

wherein the bus line connects terminals of said plurality of memory devices in a stubless configuration and an end of said bus line is terminated,

wherein at least a part of said bus line is a strip line,

wherein at least one of the plurality of memory devices and/or a register mounted on said memory module and connected to said bus line has an input terminal and an output terminal, instead of a two-way input/output terminal, for at least one two-way signal of said bus line, and

wherein said bus line has a one-way input signal line and a one-way output signal line, connected respectively to said input terminal and said output terminal, instead of a two-way signal line.

**22-24. (Canceled)**

**25. (Currently Amended)** A memory system comprising:

a ~~said~~ memory module comprising a plurality of memory devices, which share a bus line, on a board, wherein said bus line of said memory module includes a bus line for a data signal, and wherein the bus line connects terminals of said plurality of memory devices in a stubless configuration and an end of said bus line is terminated; and

a memory controller that sends a command/address signal to at least one of the plurality of memory devices of said memory module and transfers the data signal to and from said memory device,

wherein data lines between said memory controller and slots are connected in a point to point configuration.

**26. (Original)** The memory system as defined by claim 25 wherein at least a part of said data lines between said memory controller and the slots is a strip line.

**27. (Original)** The memory system as defined by claim 25 wherein a shield is provided between each two data lines.

**28. (Original)** The memory system as defined by claim 25 wherein at least one signal line, which connects said memory controller and two slots in a T-branch structure, is included.

**29. (Original)** The memory system as defined by claim 28 wherein said signal line is a command/address

signal line.

**30. (Previously Presented)** The memory system as defined by claim 25 wherein said bus line is terminated by both said memory controller and said memory module.

**31. (Original)** The memory system as defined by claim 25 wherein one channel is divided into a plurality of slots.

**32. (Original)** The memory system as defined by claim 25 wherein said memory module has a memory device, which contains a termination circuit, on a board, wherein two memory devices mounted across said board and placed in opposing positions on a front surface of said board and a back surface of said board are connected commonly to said bus line, and wherein said bus line is terminated by one of said two devices which is not accessed or driven.

**33. (Original)** The memory system as defined by claim 25 wherein a reference voltage (Vref) is generated by said memory controller and the memory device that terminates the bus line.

**34. (Previously Presented)** The memory system as defined by claim 25:

wherein said memory module is connected to a motherboard via a connector, said motherboard having said memory controller mounted thereon, and

wherein said connector is a butterfly type connector with a configuration in which said memory module is inserted in a direction parallel to a surface of said motherboard.

35. **(Previously Presented)** The memory system as defined by claim 25:

wherein said memory module is connected to a motherboard via a connector, said motherboard having said memory controller mounted thereon, and

wherein said memory module and/or said connector has cooling means.

36. **(Original)** The memory system as defined by claim 25 wherein said memory controller has a logical threshold voltage output circuit that generates a reference voltage,

wherein the reference voltage output from said logical threshold voltage output circuit is connected to said memory module via a reference voltage line,

wherein, in said memory module, an on-chip terminator on the memory device that includes a termination circuit at the end of said bus line is connected to said reference voltage line,

wherein a reference voltage terminal of the memory device connected to said bus line is connected to said reference voltage line, and

wherein said logical threshold voltage output circuit has a push-pull type driver circuit with the same configuration as that of a push-pull type driver circuit in an output circuit and an input terminal and an output terminal of said push-pull type drive circuit are connected.

37. **(Previously Presented)** The memory system as defined by claim 25 wherein said memory controller has a logical threshold voltage output circuit that generates a reference voltage,

wherein the reference voltage output from a logical threshold voltage output circuit is connected to said memory module via a reference voltage line,

wherein, in said memory module, an on-chip terminator on the memory device that

includes a termination circuit at the end of said bus line is connected to said reference voltage line,

wherein a reference voltage terminal of the memory device connected to said bus line is connected to said reference voltage line,

wherein said memory controller has an output circuit comprising an open drain type driver,

wherein a gate terminal of said open drain type driver is connected to an output terminal of a level conversion circuit that receives an internal signal and that performs level conversion,

wherein said logical threshold voltage output circuit has the level conversion circuit which has the same configuration as that of said output circuit and in which an input terminal and an output terminal are connected, and

wherein an output of said level conversion circuit is connected to a gate terminal of said open drain type driver for outputting the reference voltage.

**38. (Original)** The memory system as defined by claim 25 wherein registers are provided on a motherboard, each of said registers being connected to said bus line for performing signal conversion.

**39. (Previously Presented)** The memory system as defined by claim 25:

wherein at least one of the plurality of memory devices and/or a register mounted on said memory module and connected to said bus line has an input terminal and an output terminal, instead of a two-way input/output terminal, for at least one two-way signal of said bus line,

wherein said bus line has a one-way input signal line and a one-way output signal line connected respectively to said input terminal and said output terminal of said memory device or

said register,

wherein said memory controller on a motherboard has an output terminal and an input terminal corresponding to signals from the input terminal and the output terminal of said memory device or said register, and

wherein said output terminal and said input terminal of said memory controller are connected respectively to said input terminal and said output terminal of said memory device and/or said register each via said one-way line in a point-to-point configuration.

**40. (Previously Presented)** The memory system as defined by claim 25 wherein at least one of the plurality of memory devices and/or a register mounted on said memory module and connected to said bus line has an input terminal and an output terminal separately, instead of having one input/output terminal, for at least one two-way signal of said bus line,

wherein said bus line has a one-way input signal line and a one-way output signal line connected respectively to said input terminal and said output terminal of said memory device or said register,

wherein said memory controller on a motherboard has an output terminal and an input terminal corresponding to signals from the input terminal and the output terminal of said memory device or said register, and

wherein a daisy chain connection is made between said memory controller and the slots of a plurality of said memory modules via said one-way input signal line and output signal line.

**41. (Previously Presented)** The memory system as defined by claim 25:

wherein at least one of the plurality of memory devices and/or a register mounted on said

memory module and connected to said bus line has an input terminal and an output terminal separately, instead of having one input/output terminal, for at least one two-way signal of said bus line,

wherein said bus line has a one-way input signal line and a one-way output signal line connected respectively to said input terminal and said output terminal of said memory device or said register,

wherein said memory controller on a motherboard has an output terminal and an input terminal corresponding to signals from the input terminal and the output terminal of said memory device or said register,

wherein said output terminal or said input terminal of said memory controller is connected respectively to said input terminal or said output terminal of a memory device mounted on said memory module in a slot at a starting position and/or said register via said one-way line,

wherein, between said memory modules, the output terminal and the input terminal of said memory device in one slot and/or said register are connected respectively to the input terminal and the output terminal of said memory device in a neighboring slot and/or said register through a connector and one-way lines, and

wherein the output terminal or the input terminal of said memory device in a slot at an ending position and/or said register is connected to said input terminal or said output terminal of said memory controller via said one-way line of said motherboard.

**42. (Previously Presented)** The memory system as defined by claim 25 wherein at least one of the plurality of memory devices and/or a register mounted on said memory module and connected to said bus line differentially transmits at least one signal of said bus line to or from said memory

controller on a motherboard connected via a connector.

**43. (Previously Presented)** The memory system as defined by claim 42:

wherein, in said bus line, at least one line pair out of a plurality of line pairs, over which the signal is differentially transmitted, is composed of a first line and a second line which are complementary each other and are placed in this order in a connection from said memory controller to said connector, and

wherein the positions of the first line and the second line of said line pair are exchanged and said lines are placed in order of said second line and said first line in a connection from said connector and said memory module.

**44. (Previously Presented)** The memory system as defined by claim 42:

wherein, for a plurality of line pairs, a first line pair and a second line pair are alternately placed, said first line pair being composed of complementary signals whose positions are exchanged between a connection from said memory controller to said connector and a connection from said connector to said memory module, said second line pair being composed of complementary signals whose positions are not exchanged between the connection from said memory controller to said connector and the connection from said connector to said memory module.

**45. (Previously Presented)** The memory module as defined by claim 2, wherein the bus line is approximately parallel to a short side of the memory module.

**46. (Currently Amended)** The memory module as defined by claim 2, wherein the bus line forms a right angle with a [[the]] connector.

**47. (Previously Presented)** The memory module as defined by claim 2, wherein the terminals of the memory module are disposed on a front surface and a back surface of the memory module.

**48. (Previously Presented)** The memory system as defined by claim 25, wherein the bus line is approximately parallel to a short side of the memory module.

**49. (Currently Amended)** The memory system as defined by claim 25, wherein the bus line forms a right angle with a [[the]] connector.

**50. (Previously Presented)** The memory system as defined by claim 25, wherein the terminals of the memory module are disposed on a front surface and a back surface of the memory module.